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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): H1840

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on March 11, 2006

Signature: Winona C. Orange

Typed or printed name: Winona C. Orange

Application Number	Filed
10/791,096	3/1/2004

First Named Inventor: Ryan et al.

Art Unit	Examiner
2813	Heather Anne Doty

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 27,449
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34.

Mikio Ishimaru
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March 11, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Docket No.: H1840 ***PATENT***

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Errol Todd Ryan, et al.	: Confirmation No.:	2466
Serial No.:	10/791,096	: Art Unit:	2813
Filed:	3/1/2004	: Examiner:	Heather Anne Doty
For:	CONTACT LINER IN INTEGRATED CIRCUIT TECHNOLOGY	:	

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ARGUMENTS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

Madam:

The following Arguments are submitted under the Pre-Appeal Brief Conference Pilot Program with a Pre-Appeal Brief Request for Review and Notice of Appeal in response to the Office Action mailed December 13, 2005.

The pending claims 1,2 4-7, 9-12, 14-17, 19, and 20 are set forth in the Applicants' Amendment dated October 11, 2005.

ISSUES PRESENTED

Did the Examiner err in an attempt to create a *prima facie* case of obviousness with respect to claims 1, 2, 4-7, 9-12,14-17, 19, and 20 under 35 U.S.C. §103?

ARGUMENT

The Examiner has not established a *prima facie* case of obviousness under 35 U.S.C. §103 with respect to the pending claims. There is no disclosure, teaching, or suggestion in any of the cited references of establishing a thermal budget for forming a silicide and forming contacts within that thermal budget as claimed by Applicants. The

Examiner's assertions are contrary to the teachings of the references. This is a reversible error that will be overturned on appeal.

Claims 1, 2, and 4-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chang (U.S. Patent No. 6,858,506, hereinafter "Chang") in view of Lim (U.S. 2004/0115929, hereinafter "Lim").

Chang teaches a metal oxide transistor having a strained channel by forming a SiGe layer on the surface of a substrate and then forming a strained silicon layer over the SiGe layer. Chang does not teach the formation of an interlayer dielectric layer having contact holes formed therein, the formation of contact liners, or the formation of contacts, much less within the thermal budget for forming a silicide.

Lim teaches a method of manufacturing a semiconductor device by forming a tungsten nitride layer in contact holes using an atomic layer deposition method. There is no teaching or suggestion of the formation of a silicide, a thermal budget for the formation of a silicide, or forming the contacts within the thermal budget for the silicide.

Claims 1 and 6, as exemplified in claim 1, include the limitation not taught or suggested by Chang or Lim, taken either singly or in combination, of:

> "forming a silicide on the source/drain junctions and on the gate within a thermal budget having a temperature dependent upon the silicide metal;
> forming contact liners in the contact holes within the thermal budget for forming the silicide"

The Examiner has stated:

> "Chang teaches ... forming a nickel silicide on the source/drain junctions and on the gate (234 in Fig. 2G; column 4, line 56 - column 5, line 10) within a thermal budget having a temperature dependent upon a silicide metal..."

Applicants respectfully disagree. Chang fails to teach or suggest anything relating to a thermal budget much less forming contact liners within the thermal budget for forming a silicide as claimed by Applicants. Chang only teaches an annealing process with respect to formation of the silicide at column 4, lines 62-64:

> "After executing an annealing process, for example, at a temperature of about 400 to 800 degrees Celsius for about 20 to 60 seconds..."

Chang teaches an annealing process unrelated to, and in excess of, the thermal budget for forming a silicide. There is no teaching by Chang with respect to "a thermal budget having a temperature dependent upon the silicide metal" as claimed, and in the case of a nickel silicide having a thermal budget of about 400 °C to 450 °C, Chang teaches forming the contacts at a temperature in excess (up to 800 degrees Celsius as quoted above) of the thermal budget, and therefore teaches away from Applicants' invention.

The Examiner also has stated: "Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts."

Applicants agree that Chang fails to teach the formation of an interlayer dielectric layer, any contact holes in the interlayer dielectric, any contact liners of any type in the contact holes, much less at the thermal budget for forming the silicide as claimed by Applicants.

The Examiner also has stated:

> "Lin (sic) discloses keeping the reaction chamber at a temperature between 250 °C and 550 °C, a temperature range that overlaps with the thermal budget of nickel silicides)."

However, Lim is silent with respect to the formation of any silicide much less within the thermal budget associated with forming the silicide as claimed by Applicants. Furthermore, in the case of a nickel silicide having a thermal budget of about 400 °C to 450 °C, Lim teaches forming the contacts at a temperature in excess (up to 550°C as quoted above) of the thermal budget, and therefore teaches away from Applicants' invention.

Applicants submit that:

> "[T]he prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants' disclosure." *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Also, since Lim is silent with regard to forming contact liners in semiconductors having silicide layers, it is submitted that the proposed combination of Chang and Lim is inappropriate and without foundation, because where there is a specific hint or suggestion in a particular reference, but the references as a whole teach away from each other, the combination cannot be obvious according to the CAFC:

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> "We have noted elsewhere, as a "useful general rule," that references that teach away cannot serve to create a prima facie case of obviousness... If references taken in combination would produce a "seemingly inoperative device", we have held that such references teach away from the combination and thus cannot serve as predicates for a prima facia case of obviousness." *In re* Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)[deletion for clarity]

Claims 1 and 6 are allowable because of *In re* Vaeck, *supra* and *In re* Gordon, *supra*.

Claims 9, 11, 12, 15-17, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chang (U.S. Patent No. 6,858,506, hereinafter "Chang") in view of Lim (U.S. 2004/0115929, hereinafter "Lim") as applied to claims 6, 11, and 17 above, and further in view of Tseng (U.S. 2005/0035460, hereinafter "Tseng").

Chang and Lim have been summarized above.

Tseng teaches a damascene structure and process in which a buffer metal layer is provided on an exposed contact region. A conductor is provided on the buffer metal layer.

With regard to claim 11, claim 11 includes the limitation not taught or suggested by Chang, Lim, or Tseng taken either singly or in combination, of:

> "an ultra-thin silicide on the source/drain junctions and on the gate"

The Examiner has reiterated the reasons for rejection of claims 1 and 6 above, and also stated with regard to Tseng:

> Tseng teaches forming nickel silicide layers with a thickness of 50 - 350 A (paragraph 0037), within the limits indicated in the instant specification on page 8, line 4 of "not more than 50 A thickness. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the nickel silicide layer ultra-thin, as taught by Tseng."

However, Chang is silent with respect to the thickness of the silicide (see for example, column 4, lines 56-67). Also as stated above, Lim is silent with respect to the formation of any silicide much less an ultra-thin silicide as claimed by Applicants. Accordingly, it is submitted that claim 11 is allowable because of *In re* Vaeck, *supra* and *In re* Gordon, *supra*.

With regard to claim 17, claim 17 includes the limitation not taught or suggested by Chang, Lim, or Tseng taken either singly or in combination, of:

"an ultra-thin thickness of a nickel silicide on the source/drain junctions and on the gate"

The Examiner has stated the same basis of rejection as set forth with respect to claim 11.

Accordingly, Applicants submit that claim 17 is allowable over Chang in view of Lim, and in further view of Tseng taken either singly or in combination for the reasons set forth above with regard to claim 11 because of *In re* Vaeck, *supra* and *In re* Gordon, *supra*.

Claims 10, 14 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chang (U.S. Patent No. 6,858,506, hereinafter "Chang") in view of Lim (U.S. 2004/0115929, hereinafter "Lim") as applied to claim 6 above, and further in view of Tseng (U.S. 2005/0035460, hereinafter "Tseng") and Wolf et al. (Silicon Processing for the VLSI Era, Vol. 1, hereinafter "Wolf").

Claims 2, 4, 5, 7, 9, 10, 12, 14-16, 19, and 20 depend upon claims 1, 6, 11, and 17 and are believed to be allowable because of *In re* Vaeck, *supra* and *In re* Gordon, *supra* for the reasons set forth above with regard to claims 1, 6, 11, and 17 since they contains all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

CONCLUSION

It is respectfully submitted that the Examiner erred in the attempt to create *prima facie* cases of obviousness under 35 U.S.C. §103 by citing references that are not properly combined and even if combined do not disclose, teach, or suggest all the limitations of Applicants' invention.

In view of the above, it is submitted that claims 1, 2, 4-7, 9-12, 14-17, 19, and 20 are in condition for allowance and such action at an early date is solicited.

Respectfully submitted,

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